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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year I Semester (R16) Regular Examinations November 2017
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units 5 X 12 = 60 Marks)

UNIT-I

- 1 a Convert $(2AC5.D)_{16}$ to binary and then to octal. 6M
 b Explain how transfer of information will be done among registers. 6M

OR

- 2 a Simplify the following Boolean expressions
 (i) $A'C' + ABC + AC'$ 8M
 (ii) $(A'+C)(A'+C')(A+B+C'D)$
 b Obtain the dual of the function $F = AB + (AC)'AB'C$ 4M

UNIT-II

- 3 a Simplify the following Boolean expression using k-map 7M
 $F(w,x,y,z) = \Sigma (1,3,7,11,15) + d (0,2,5)$
 b Implement EX-OR gate using NOR gates only. 5M

OR

- 4 a Simplify using k-map to obtain a minimum POS expression
 $(A'+B'+C+D)(A+B'+C+D)(A+B+C+D')(A+B+C'+D')(A'+B+C+D')$ 9M
 $(A+B+C'+D)$
 b Realize the above result using the basic gates. 3M

UNIT-III

- 5 a What is full adder? With necessary derivations implement the full adder circuit. 6M
 b Design a combinational circuit with 4 inputs A,B,C,D. The output Y goes HIGH if and only if A and C inputs goes HIGH. Draw the truth table. 6M
 Minimize the Boolean unction using K-map . Draw the circuit diagram.

OR

- 6 a What is decoder? Explain 2 to 4 line decoder with truth table and draw the circuit. 6M
 b Explain 4:1 multiplexer with truth table and draw the logic diagram. 6M

UNIT-IV

- 7 a Convert the SR flipflop to T flipflop 7M
b Explain JK flipflop 5M

OR

- 8 a Explain 4-bit ring counter with suitable sketches. 6M
b Design mod-6 ripple counter using T-flipflops. 6M

UNIT-V

- 9 a. Differentiate Moore and Mealy circuit models 3M
b. Explain Moore model. 9M

OR

- 10 Realize the following four Boolean functions using PAL
(i) $F_1(w,x,y,z) = \Sigma m(0,1,2,3,7,9,11)$
(ii) $F_2(w,x,y,z) = \Sigma m(0,1,2,3,10,12,14)$
(iii) $F_3(w,x,y,z) = \Sigma m(0,1,2,3,10,13,15)$
(iv) $F_4(w,x,y,z) = \Sigma m(4,5,6,7,9,15)$ 12M

***** END *****